## REMARKS

Claims 1-8, 10-12, 14-23, and 25-27 are presented for examination. Claims 1, 10, 23, and 26 are currently amended. Claims 9, 13, and 24 have previously been canceled. No new claims have been added.

In the Office Action Claims 1-5, 7, 8, 23, and 25 were rejected under 35 USC § 102(b) as being anticipated by Wilford (U.S. 6,020,762). Claims 6, 10-12, 14-22, and 26-27 were rejected under 35 USC 103(a) as being unpatentable over Wilford.

Wilford

Claims 1, 10, 23, and 26 are currently amended, support for which can be found in the specification as filed, for example, at paragraphs [0037], [0048] - [0050], [0058], and [0064] - [0065]; and in Figures 1A, 1B, 3, and 4.

With regard to Wilford, Applicants note that Wilford admits Figure 1 as prior art (col. 1, lines 24-37); and admits that Figure 4 is the same as Figure 1 unless a low voltage signal is present (at line 141) to assist transistor 107 (col. 2, line 18-36). Wilford states that, otherwise, Figure 4 is the same as Figure 1 (col.3, line 66 - col. 4, line5 and col. 4, lines 53-54). Moreover, Wilford teaches that transistor 107 is much smaller than transistor 103 (col. 3, lines 58-65) and Applicants therefore respectfully submit that the Office action assertion that Wilford is silent about size for transistors and "thus assume that 105=109 in size and 107=103 in size" is not justified with regard to claims 7 and 12.

Contrary to teaching adjusting the size of transistors, Wilford teaches providing additional circuit elements (e.g., transistor 143) for compensating for the size of transistor 107 and thus teaches away from the present invention's use of size to achieve desired operating characteristics as in claims 6, 7, 10-12, 18,

and 27. Therefore, Applicants submit that the rejections to those claims as anticipated or made obvious by Wilford in regard to transistor size should be withdrawn.

Wilford teaches a level shifter or voltage translator (FIG. 6, element 307) that preserves timing relationships of an input signal. Indeed, Wilford teaches complementary signals at outputs 124, 123 that are inverses of each other, as shown at $V_{out1}$, $V_{out2}$ (FIG. 5). The complementary signals are provided at outputs 124, 123 (FIG. 4) to drive two distinct separate loads as shown at CLOAD1 and CLOAD2 (FIG. 1, in light of col. 4, lines 53-54). In order to provide complementary signals at outputs 124, 123, Wilford's buffer 111 providing output 124, and buffer 113 providing output 123, are both inverters and each inverts the output that it receives from the cross-coupled inverters (105, 107, 109, 103). Wilford teaches to keep the two outputs as close to complementary as possible so that introduction of a timing delay as shown at FIG. 3 (col. 2, lines 3-8) is presented as undesirable and Wilford teaches to keep the two outputs as nearly complementary as possible as shown at FIG. 5 (col. 5, lines 18-26). If the outputs of FIG. 5 were to be applied to a driver such as that shown at Figure 3 of the present invention, both driver transistors 330, 340 would be off for half the signal cycle (providing no current at output 350) and then both transistors would be on for the remaining half of the signal cycle, which condition is known as a "crowbar" current flowing through the transistors, effectively shorting the power supply to ground through the driver transistors.

Thus, the circuit of Wilford teaches away from a break before make predriver having buffer connections for a driver to drive a single load as in claim 1 (as amended). The timing relationships claimed in claims 1 and 26 give rise to predriver output signals (as illustrated by Figure 1B) in which, contrary to the complementary signals of Wilford, the predriver output signals are in-phase most of the time. For example, as shown in Figure 1B, the two output signals are only out of phase as indicated by the cross-hatched areas in Figure 1B. (In Figure 1B

the first output signal has rising edge 210 and falling edge 240, while the second output signal has rising edge 220 and falling edge 230.)

Moreover, the buffers of Wilford, in which each comprises a single inverter and thus preserves the complementary phase relationship of the two outputs of the cross-coupled inverters, teach away from the buffers as claimed in claims 10 and 23 (as amended) in which one of the two cross-coupled inverter outputs is inverted and the other is not, thus changing the complementary phase relationship to an in-phase relationship that provides the break-before-make timing claimed in claims 10 and 23. So, for example, a driver connected to the buffer outputs would have either a first transistor on and second transistor off or a first transistor off and second transistor on, with both transistors off during the rising or falling transitions and avoiding the "crowbar" condition of having both transistors on, contrary to the principles of operation taught by Wilford in which a driver connected to the buffer outputs would have either both transistors off or both transistors on. Thus, the buffer outputs taught by Wilford would be useless for operating a driver as taught by the present invention, for example, at claim 1.

Therefore, Applicants submit that Wilford neither anticipates nor makes obvious the present invention as claimed by the amended claims and that the section 102 and 103 rejections should be withdrawn.

## Conclusion

In light of the arguments and amendments presented herein, the Applicants respectfully submit that all pending claims are in condition for allowance. Accordingly, reconsideration and allowance of this Application is earnestly solicited. Should any issues remain unresolved, the Examiner is encouraged to telephone the undersigned at the number provided below.

Respectfully submitted,

Dated: February 22, 2006 By: _____

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